32. (New) A process as claimed in claim 31 wherein said vertical component defines a localized thick region in the layer of conductive material.

33. (New) A process for making a semiconductor device comprising:
forming a layer of conductive material having a topography that includes a spacer;
forming a contact disposed adjacent to and contacting said spacer.

34. (New) A process as claimed in claim 33 further comprising forming a structure having an opening therein under said conductive layer and filing said opening with said conductive material to form said spacer.

35. (New) A process for making a semiconductor device having an improved contact to a conductive layer comprising:

providing a first layer of material and forming an opening therein, said opening including sidewalls;

forming a layer of a first conductive material on said first layer of material and along the surfaces of said sidewalls of said opening to form a localized thick region, wherein said first conductive material forms spacers on said sidewalls;

forming an overlayer of material on said layer of said first conductive material;

forming a contact hole in said overlayer which communicates with said layer of said first conductive material; and

substantially filling said contact hole in said overlayer with a second conductive material which differs in composition from said first conductive layer and which contacts at least said spacers.

36. (New) A process as claimed in claim 35 in which said first layer and said overlayer comprise insulating materials.

37. (New) A process for making a semiconductor device having an improved contact to a conductive layer comprising:

providing a first layer of and forming an opening therein, said opening including sidewalls;

forming a layer of a first conductive material on said first layer of material and along the surfaces of said sidewalls of said opening to form a localized thick region, said first layer of conductive material comprised of polysilicon;

forming an overlayer of material on said layer of said first conductive material;

forming a contact hole in said overlayer which communicates with said layer of said first conductive material;

substantially filling said contact hole in said overlayer with a second conductive material which differs in composition from said first conductive layer and which contacts said first conductive material, said second conductive material comprised of metal.

38. (New) A process as claimed in claim 37 in which said first layer comprises silicon dioxide said overlayer comprises boro-phospho-silicate glass.

39. (New) A process as claimed in claim 37 wherein said contact hole is positioned directly above said opening and said thick region.

REMARKS

The Office Action in the parent application rejected claims 21-30. Claims 21-25 were rejected under 35 U.S.C. 102(a) as being anticipated by Jost et al, U.S. Patent No. 5,739,068, hereinafter referred to as Jost. However, Applicant believes that the first ground was a typographical error and that the Examiner intended it to be a rejection under 35 U.S.C. 102(e) because Jost issued after Applicants' filing date. Claims 26-30 were rejected under 35 U.S.C. 103(a) as unpatentable over Jost.